UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,734,510 B2
DATED : May 11, 2004
INVENTOR(S) : Leonard Forbes et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 3,
Line 17, "conducing" should read -- conducting --.

Column 7,
Line 60, claim 1 should read:

1. A semiconductor device comprising:

a substrate having at least two spaced doped source/drain regions, said source/drain regions defining a channel region therebetween; and

a transistor gate over said substrate and wholly between said spaced doped source/drain regions, said transistor gate having one first gate electrode of a first conductivity type and two second gate electrodes of a second conductivity type, wherein said two second gate electrodes are provided on either side of said first gate electrode and are separated from said first gate electrode by an insulating dielectric layer.

Column 9,
Line 47, claim 32 should read:

32. A semiconductor device, comprising:

a semiconductor substrate, said substrate having at least two separated doped source/drain regions;

three gate electrodes over said substrate and at least partially between said source/drain regions, including a center gate electrode of P+ type conductivity and two adjacent outer gate electrodes of N+ type conductivity;

a gate dielectric separating said three gate electrodes from said substrate;

a thin dielectric layer separating said outer gate electrodes from said center gate electrode;

a first conductive cap layer over said center gate electrode and a second conductive cap layer electrically connecting said outer gate electrodes; and

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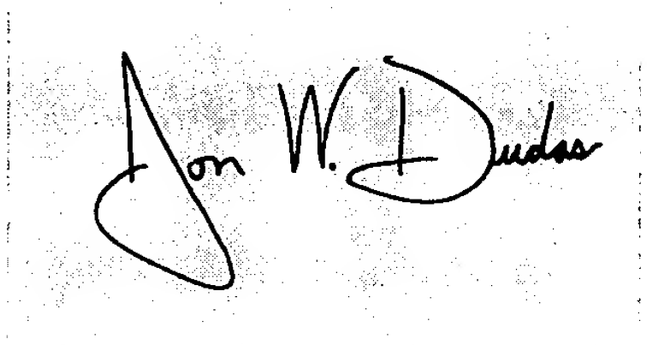
Column 9 (cont'd),

insulating sidewalls adjacent to said conductive cap layer and said outer gate electrodes.

Signed and Sealed this

First Day of November, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office